

Fig.1

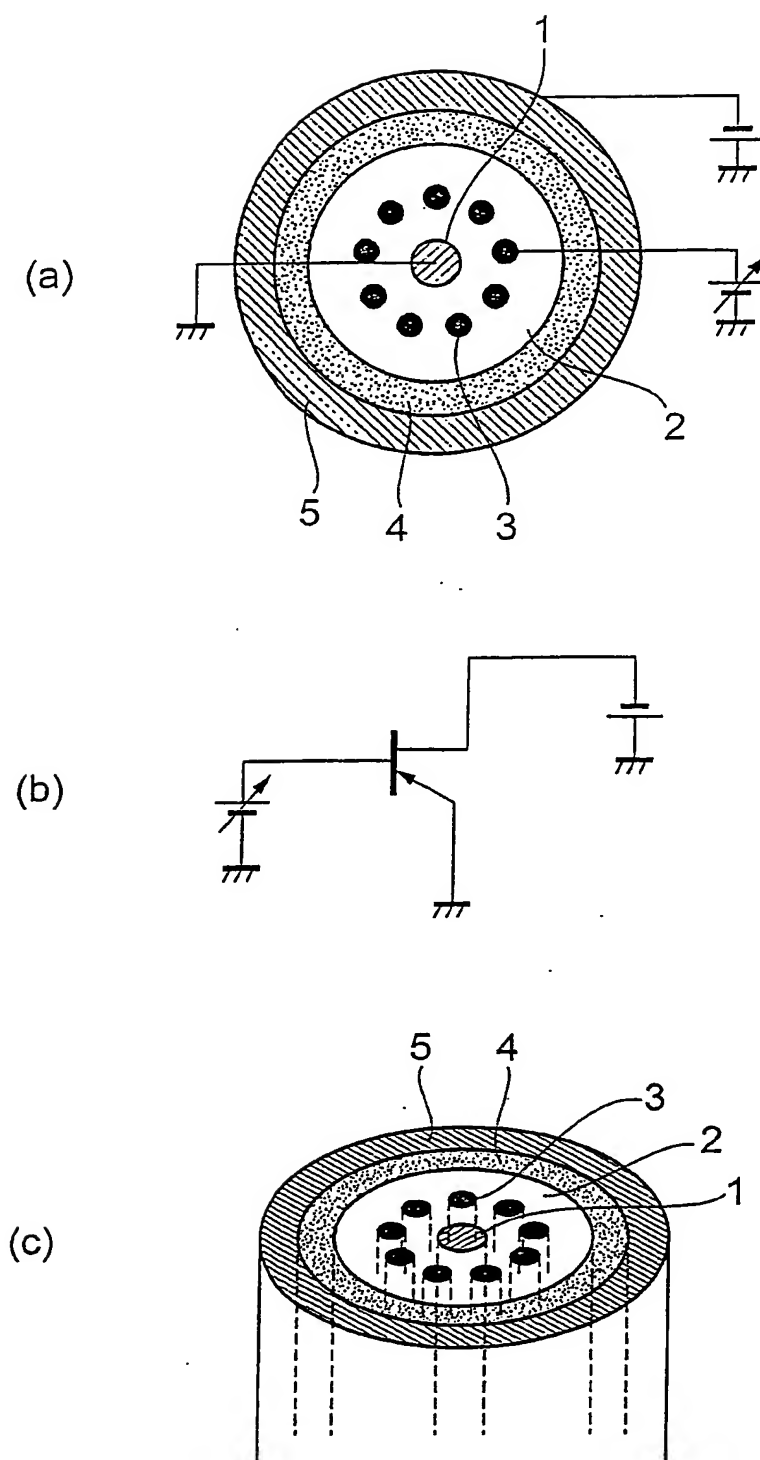


Fig.2

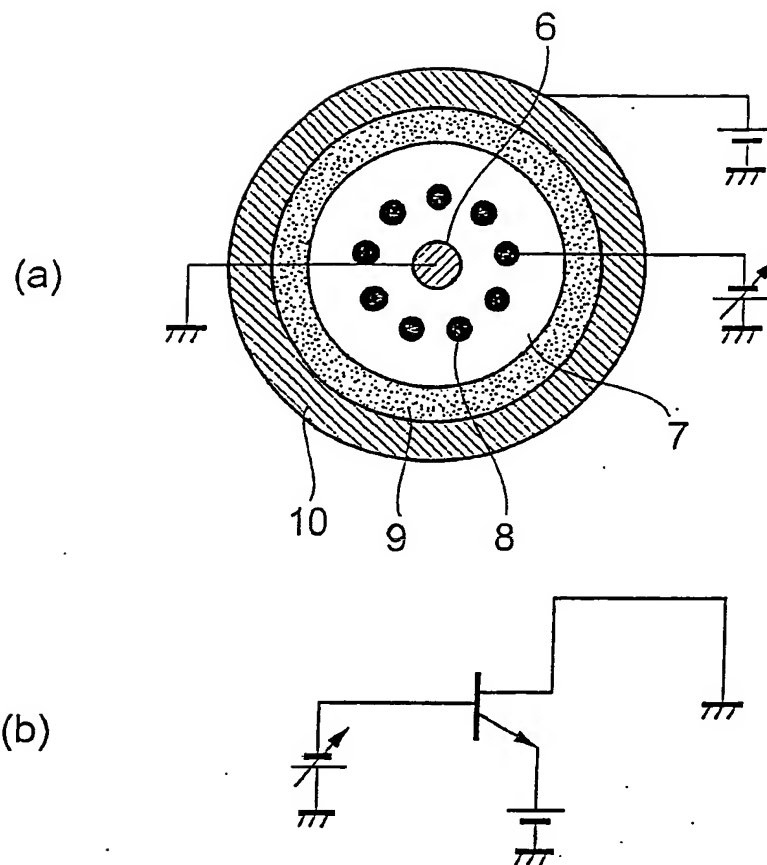


Fig.3

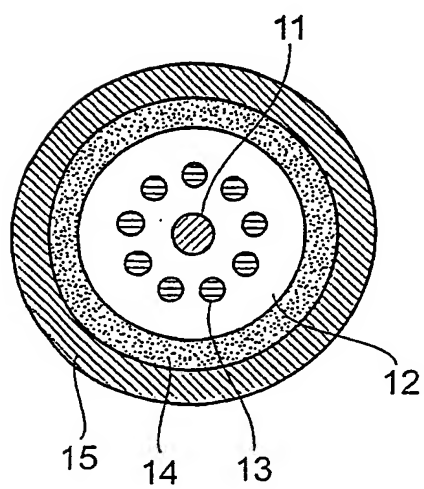


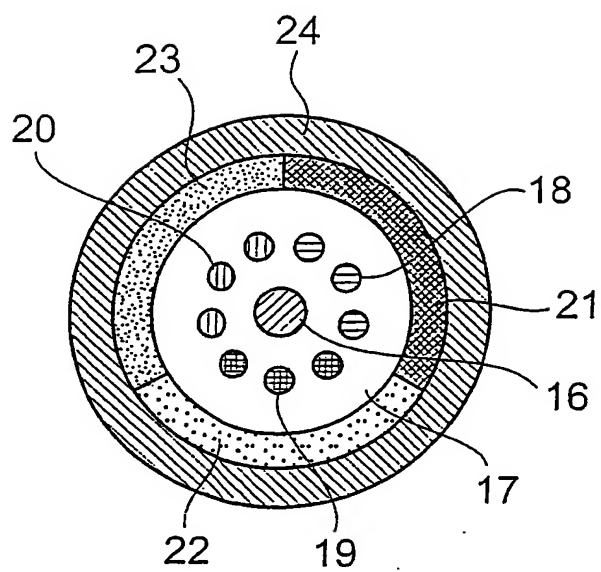
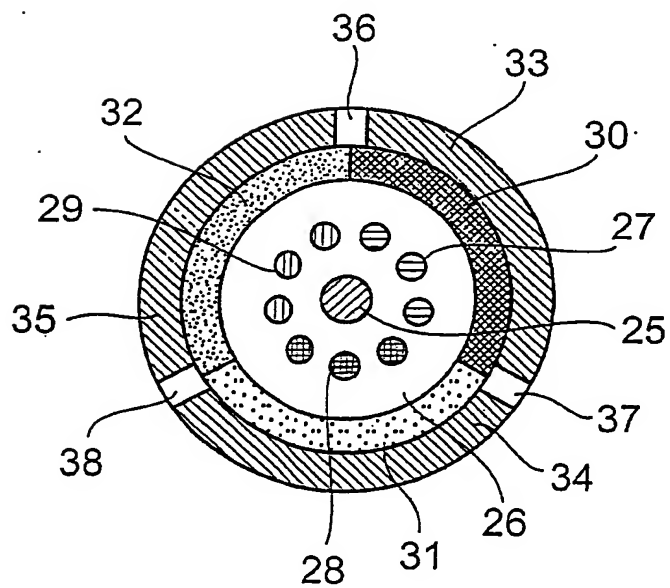
Fig.4**Fig.5**

Fig.6

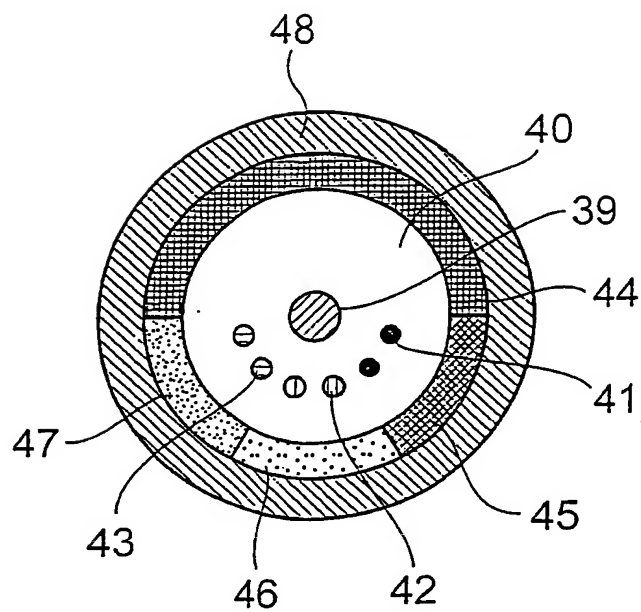


Fig.7

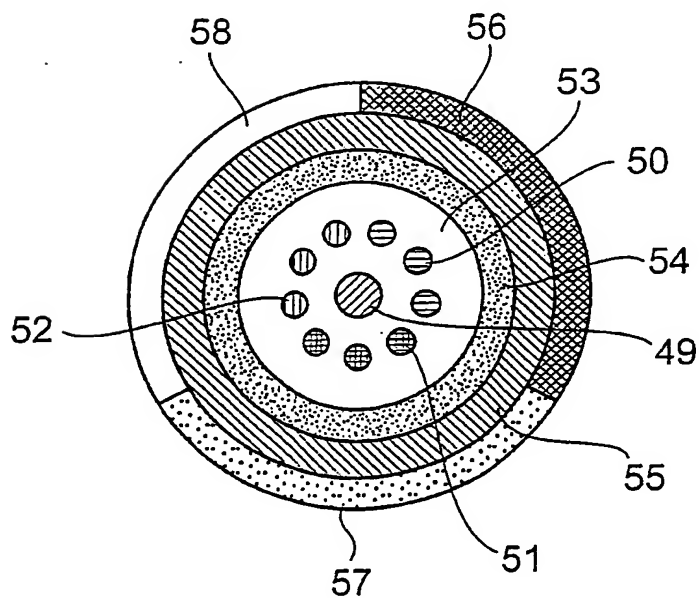


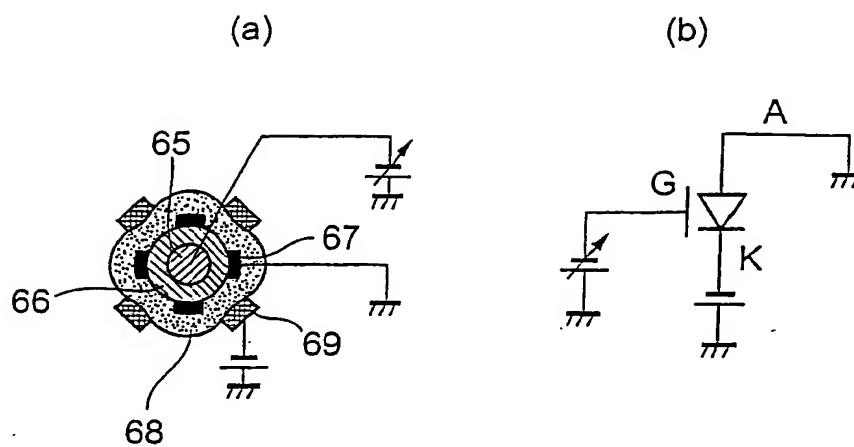
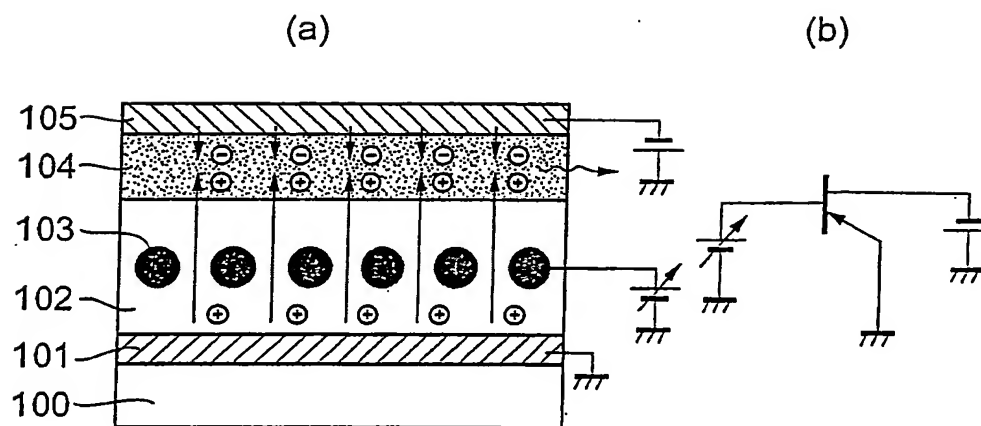
Fig.8**Fig.9**

Fig.10

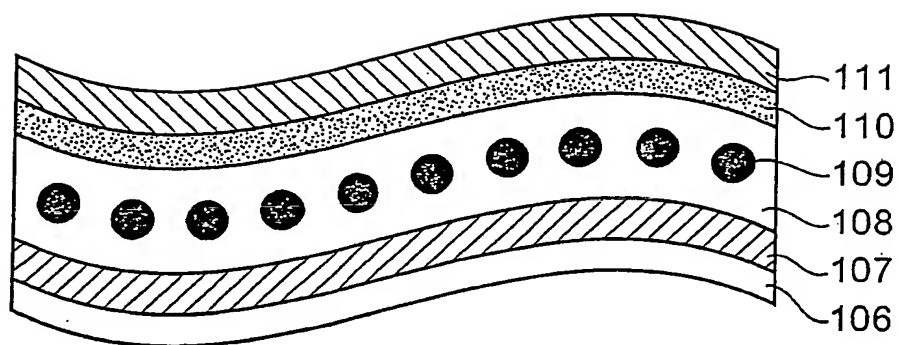


Fig.11

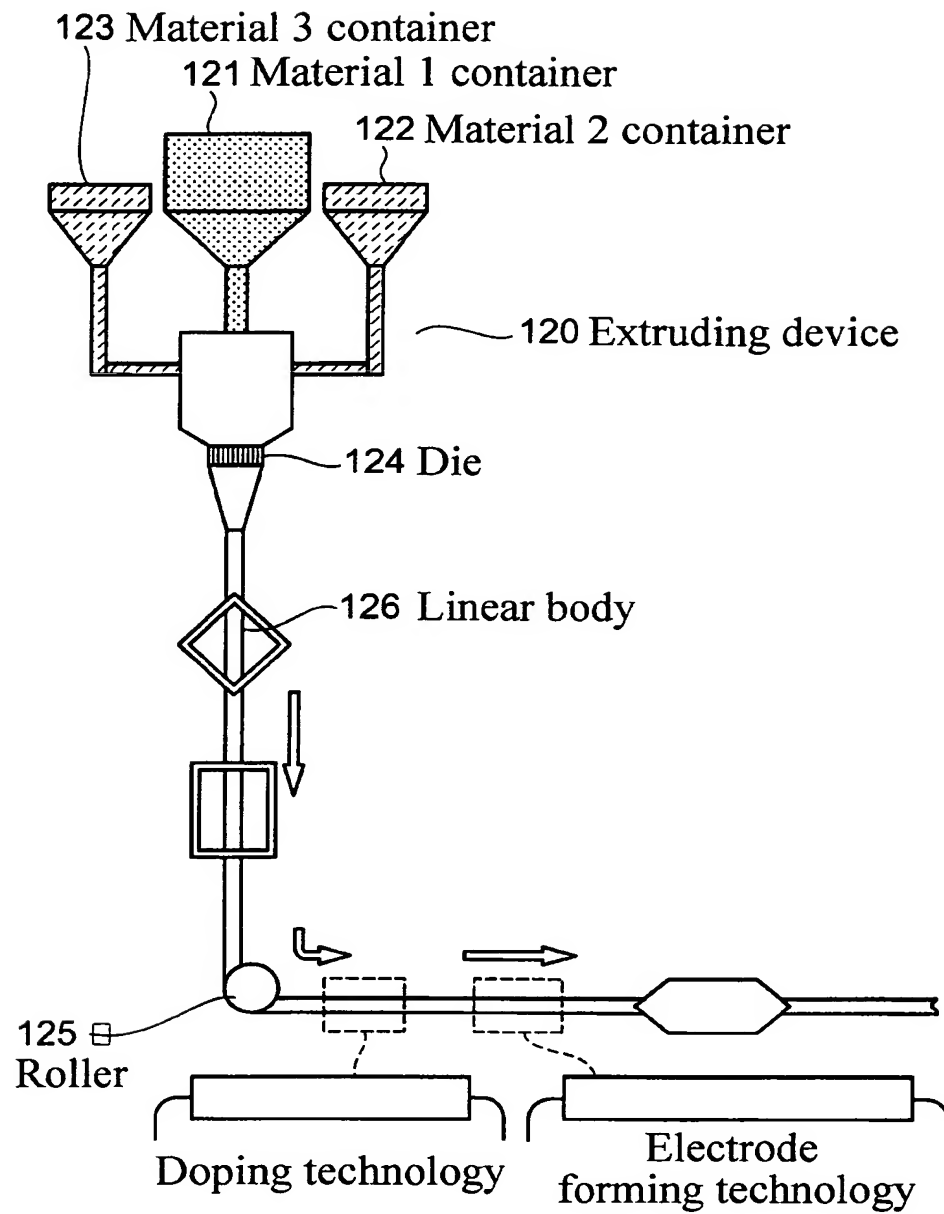


Fig.12

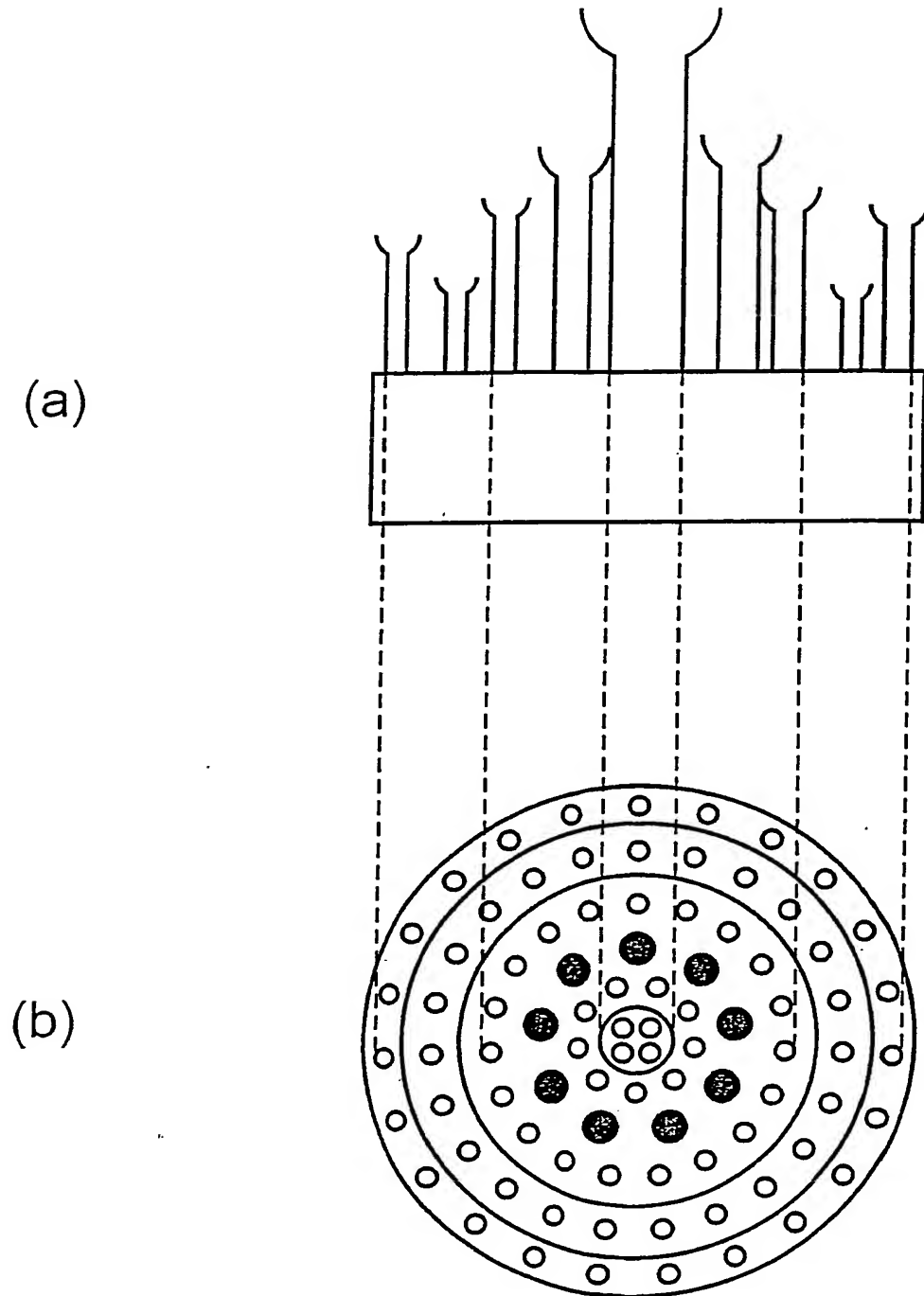


Fig.13

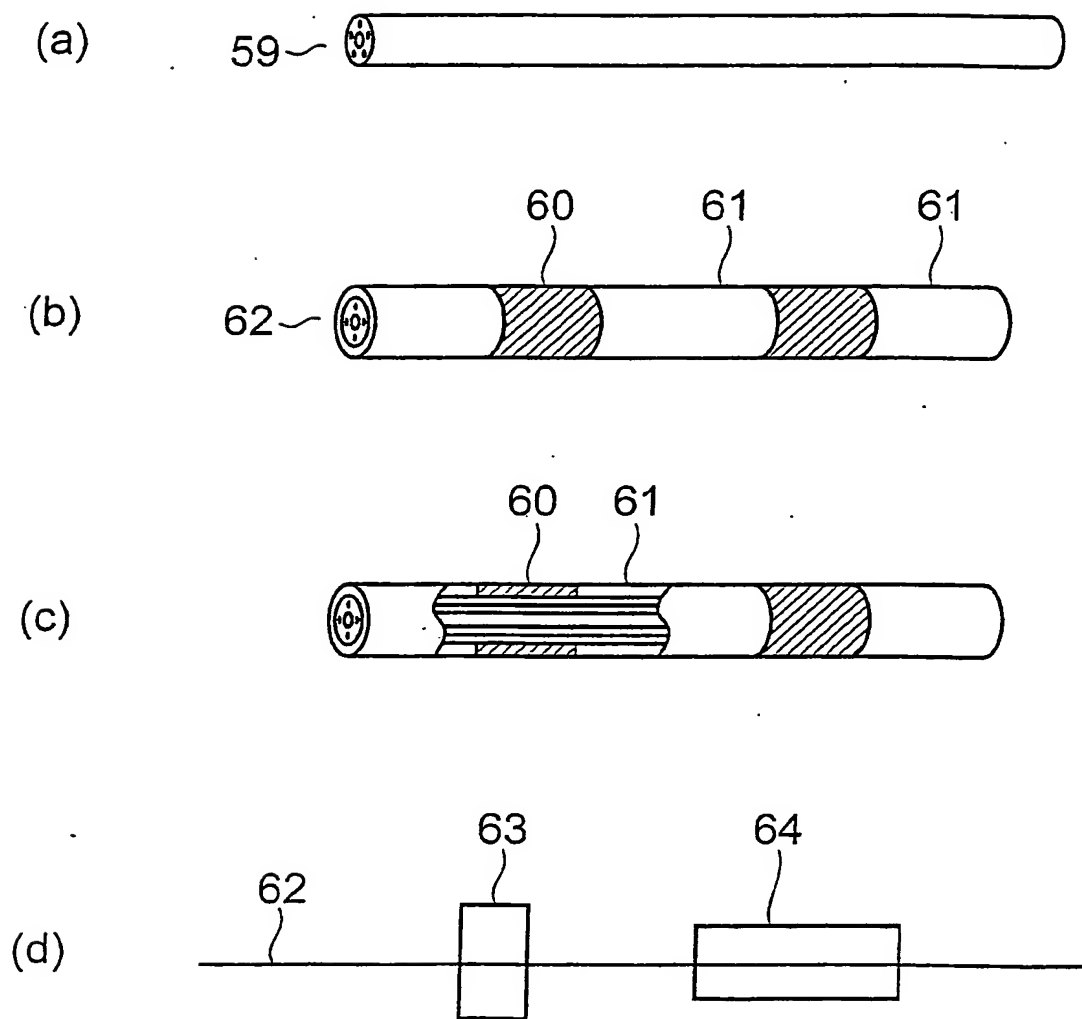


Fig.14

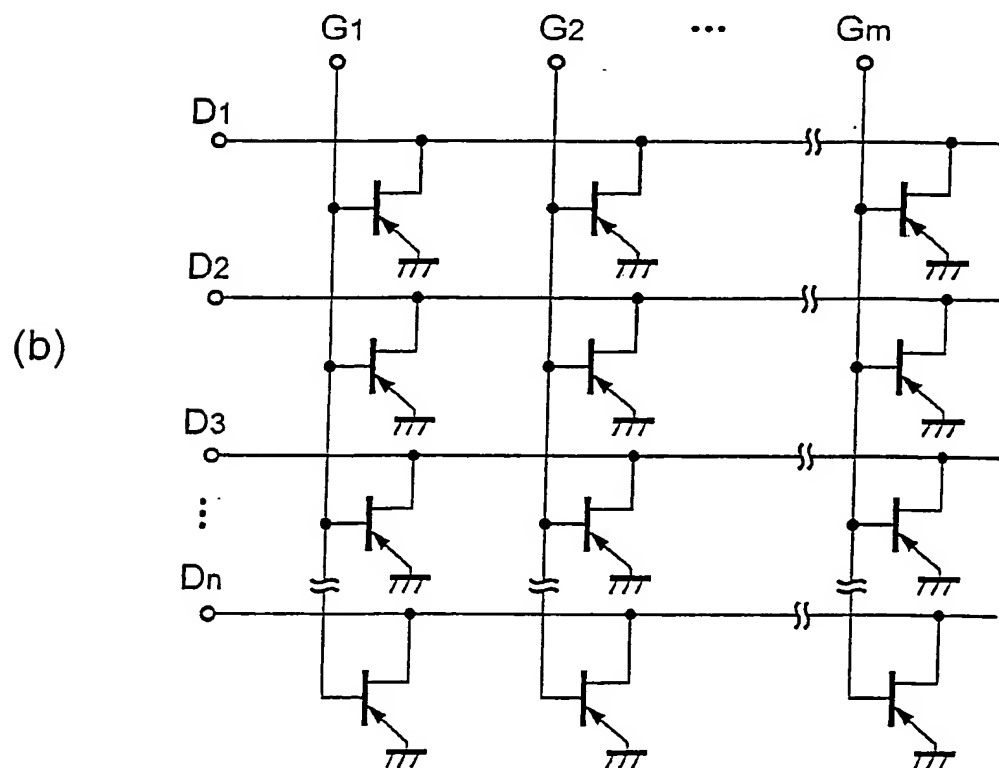
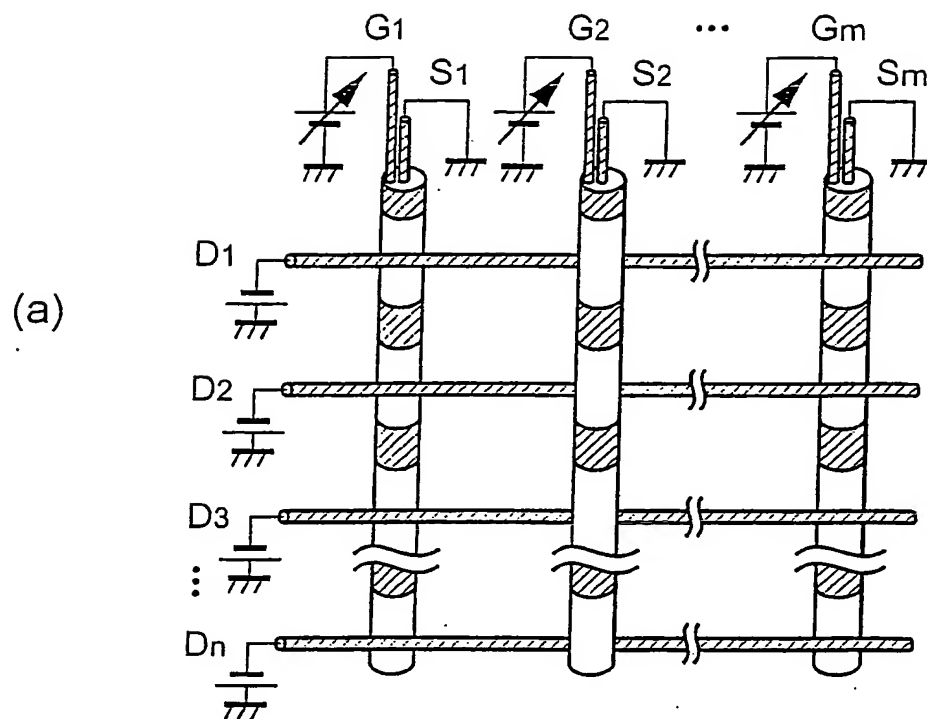


Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 1001, a first insulating layer 1002, a second insulating layer 1003, a third insulating layer 1004, and a fourth insulating layer 1005. A gate structure 1006 is formed on the surface of the substrate 1001, comprising a gate electrode 1007 and a gate insulating layer 1008. A channel region 1009 is formed in the substrate 1001. The dimensions L1 and L2 are indicated.

A cross-sectional view of a semiconductor device. The device consists of a substrate with several layers. From bottom to top, the layers are labeled 1008, 1009, 1010, 1011, and 1012. Layer 1008 is the base substrate. Layer 1009 is a thin layer above 1008. Layer 1010 is a thicker layer with diagonal hatching. Layer 1011 is a thin layer above 1010. Layer 1012 is the topmost layer, which is patterned into a series of rectangular blocks. In the center of the device, there is a region labeled 1013. This region contains a layer labeled 1014, which is a rectangular block with a stippled pattern, situated within the 1011 layer.

A cross-sectional view of a semiconductor device. The device consists of a substrate 1015 at the bottom, followed by a series of layers: 1016, 1017, 1018, 1019, 1020, 1021, and 1022. A central structure 1024 is formed within the layers 1018 and 1019. A top layer 1023 is formed over the device, and a contact pad 1025 is formed on the top layer 1023.

Fig.18

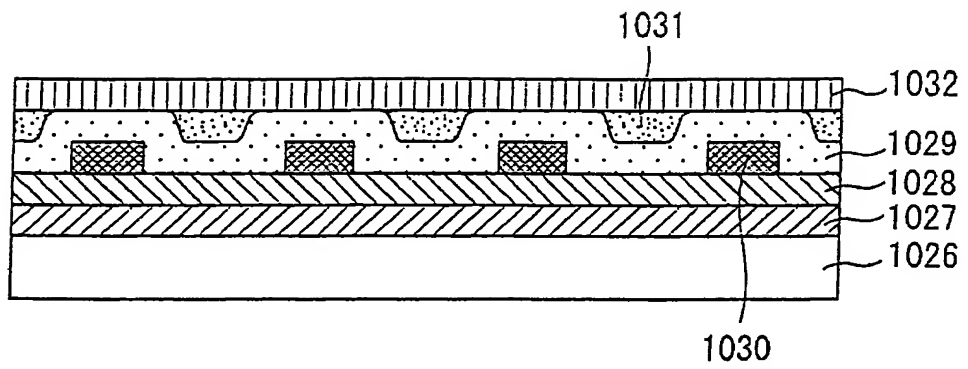


Fig.19

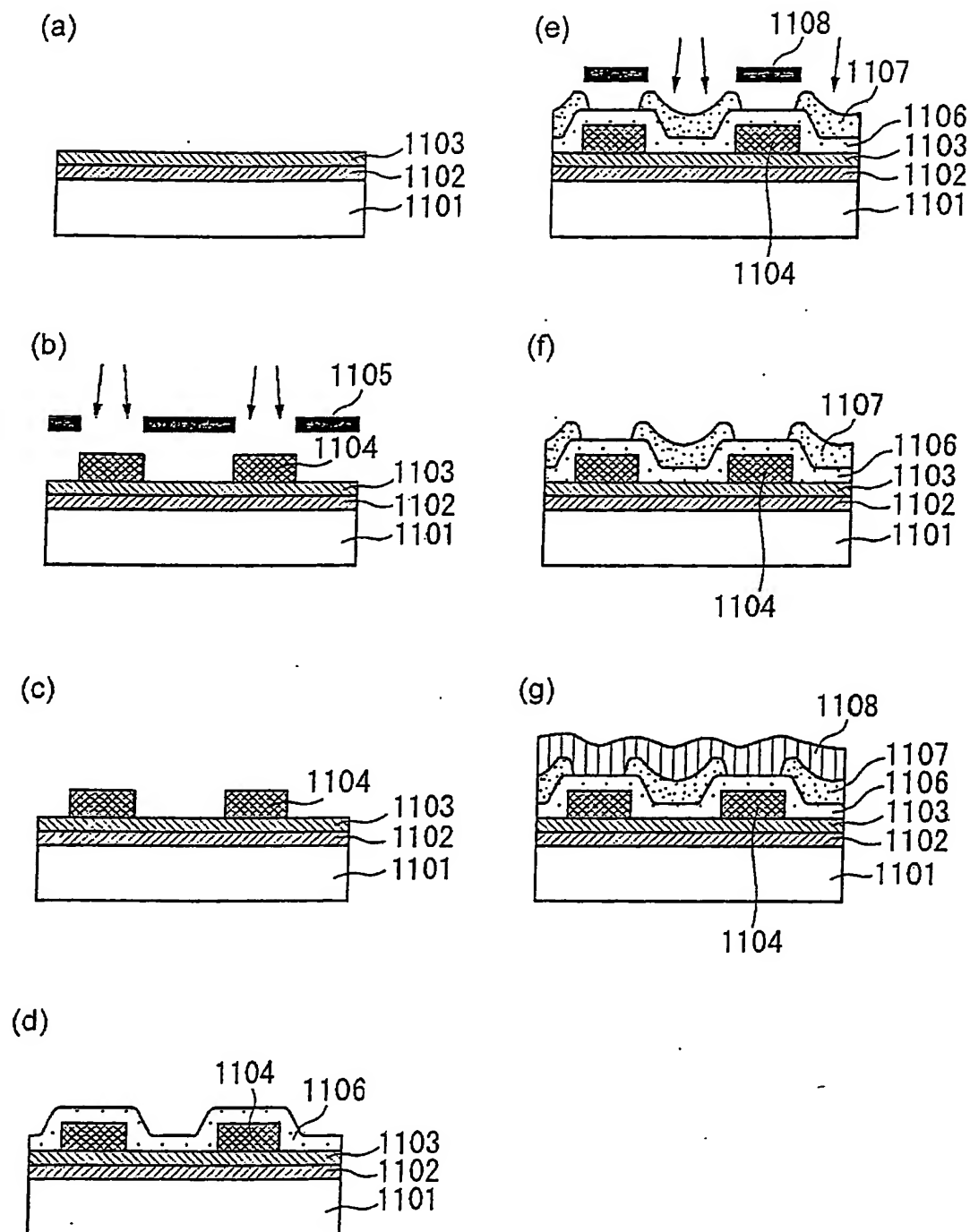


Fig.20

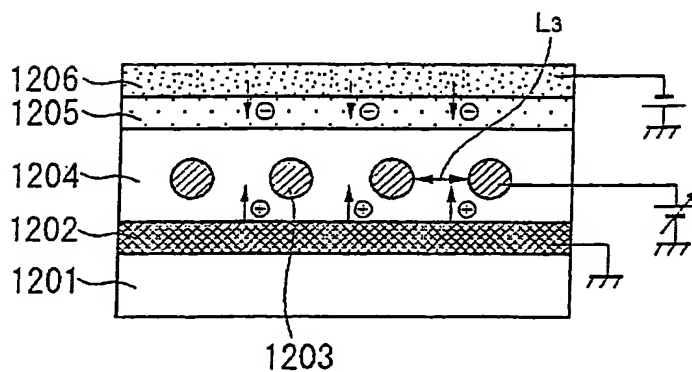


Fig.21

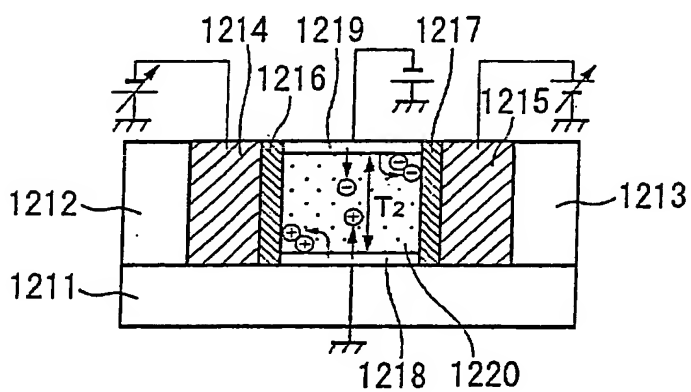


Fig.22

